

1 CLAIMS

1. In a memory component having a memory component capacitance and memory component operational characteristics, a  
5 diffusion replica delay circuit, comprising:
  - a. a diffusion replica capacitor, coupled to the memory component, and capable of storing a predetermined replica charge representative of a selected memory component operational characteristic, and
  - 10 b. a diffusion replica transistor, coupled with the diffusion replica capacitor, coupled between the diffusion replica capacitor and a charge sink, the transistor being disposed to control the magnitude of the predetermined replica charge.
- 15 2. The diffusion replica delay circuit of Claim 1, wherein the memory component includes a dummy cell with a dummy bit line and a plurality of wordlines, the diffusion replica capacitor being coupled to the split dummy bit line and a  
20 limited number of wordlines.
3. The diffusion replica delay circuit of Claim 2, wherein the diffusion replica capacitor is coupled to one wordline.
- 25 4. The diffusion replica delay circuit of Claim 1, wherein the memory component includes a plurality of access transistors having an access chain characteristic, and the diffusion replica transistor is disposed to be representative of the access chain characteristic.
- 30 5. The diffusion replica delay circuit of Claim 2, wherein the memory component includes a plurality of access transistors having an access chain characteristic, and the diffusion replica transistor is disposed to be representative of the  
35 access chain characteristic.

- 1     6.    The diffusion replica delay circuit of Claim 3, wherein the  
         selected memory component operational characteristic is a  
         dummy bitline capacitance of a bitline coupled to the  
         diffusion replica delay circuit, and the diffusion replica  
5       capacitance is substantially matched to the dummy bitline  
         capacitance.
7.    The diffusion replica delay circuit of Claim 6, wherein the  
         diffusion replica capacitance is substantially a  
10       predetermined fraction of the dummy bitline capacitance.
8.    The diffusion replica delay circuit of Claim 6, wherein the  
         dummy cell is coupled with a memory cell having local  
         bitlines and local wordlines, and the diffusion replica  
15       delay circuit provides a limited voltage swing signal to at  
         least one of the local bitlines and the local wordlines.
9.    The diffusion replica delay circuit of Claim 6, comprising  
         dummy cells operably coupled with a selected wordline  
20       decoder and a selected sense amplifier.
10.   The diffusion replica delay circuit of Claim 9, wherein  
         dummy cells are selectively coupled with memory cells, each  
         having local bitlines and local wordlines, and the  
25       diffusion replica delay circuit provides a limited voltage  
         swing signal to at least one of the local bitlines and the  
         local wordlines.
11.   The diffusion replica delay circuit of Claim 10, wherein  
30       the dummy cells comprise split dummy bit lines.